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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,415	02/05/2002	Ji Ung Lee	MI30-068	5182

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EXAMINER	
FULK, STEVEN J	
ART UNIT	PAPER NUMBER
2891	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/072,415	LEE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *74,75,77,78,102-106,108,109,111,113,118 and 120* is/are allowed.

6)☒ Claim(s) *79,80,83-85,88,89,92-94,96,114,116,121-127 and 130* is/are rejected.

7)☒ Claim(s) *81,82,86,128,129 and 131* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 74,75,77-86,88,89,92-94,96,102-106,108,109,111,113,114,116,118 and 120-131.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed January 8, 2007, which amends claim 93 and adds claims 123-131, has been entered. Claims 74-75, 77-86, 88-89, 92-94, 96, 102-106, 108-109, 111, 113-114, 116, 118 and 120-131 are currently pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 79 is rejected under 35 U.S.C. 102(e) as being anticipated by Hofmann et al. '605.

Hofmann et al. discloses a field effect transistor fabrication method (col. 7, lines 35-50) comprising providing semiconductive material (fig. 3, 14a) including a channel region (region under gate 17a); providing a plurality of semiconductive regions (19a/b) adjacent to the channel region of the semiconductive material, wherein at least one of the semiconductor regions comprises an emitter (13a); and self-aligning a gate with the semiconductive regions after providing the semiconductive regions (col. 8, line 65 - col. 9, line 6).

4. Claims 79-80, 83-85, 88-89, 92, 116, 121 and 123-127 are rejected under 35 U.S.C. 102(e) as being anticipated by Itoh et al. '107.

a. Regarding claims 79, 80 and 123-127, Itoh et al. discloses a field effect transistor fabrication method comprising providing a thin film semiconductive material including a channel region (fig. 7, channel portion of layer 5); providing a plurality of semiconductive regions (regions of layer 5 adjacent to channel region) adjacent to the channel region of the semiconductive material, wherein at least one of the semiconductor regions comprises an emitter (9); and self-aligning a gate with the semiconductive regions after providing the semiconductive regions to form a transistor (fig. 7, control gate 3 is self aligned to opening in film 11) comprising the gate and the semiconductive regions which are adjacent to opposing sides of the channel region, one of which is not an emitter (); the gate intermediate the semiconductive regions, wherein the gate is configured to control a flow of electrons intermediate the semiconductive regions ();

b. Regarding claims 83-85, 88, and 121, Itoh et al. discloses a field emission device fabrication method comprising providing a thin film semiconductor material (fig. 1, 5); providing a plurality of semiconductive regions adjacent to the semiconductive material (regions of layer 5 adjacent to channel region), and wherein the providing the semiconductive region comprises providing one of the semiconductive regions comprising a plurality of emitters (fig. 1, 9; fig. 2, 9); providing a gate intermediate the semiconductive regions (fig. 1, 3), wherein providing the semiconductive

regions and the gate comprise forming a field effect transistor (fig. 1); wherein the gate is provided about one of the emitters (fig. 1, 7); and wherein the plurality of emitters are electrically coupled with a single one of another of the semiconductor regions via the gate comprising a single gate electrode (fig 1, emitters 9 coupled to region 4 via channel/gate 3).

c. Regarding claims 89 and 92, Itoh et al. discloses a field emission device operational method comprising providing a plurality of semiconductive regions (fig. 1, regions of layer 5 adjacent to channel region) adjacent to a thin film semiconductive layer comprising a channel region (fig. 1, channel region of layer 5), and wherein at least one of the semiconductive regions comprises an emitter (fig. 1, 9); controlling current flow intermediate the semiconductive regions within the channel region and controlling emission of electrons from the field emitter using a gate intermediate the semiconductive regions (fig. 1, 3; col. 6, lines 13-24, current control electrode); and configuring the gate and the semiconductor regions to form a field effect transistor (fig. 1).

d. Regarding claim 116, Itoh et al. discloses a field effect transistor fabrication method comprising providing semiconductive material including a channel region (fig. 1, channel region of layer 5); providing a source semiconductive region (4) and a drain semiconductive region (region of layer 5 with emitters 9) adjacent to the channel region of the semiconductive material; and wherein the providing the drain semiconductive region comprises providing a plurality of emitters (fig. 1, 9; fig. 2, 9); providing a

gate dielectric material (fig. 1, 6) over the channel region; and providing a gate (7) over the gate dielectric material and the channel region.

5. Claims 93-94, 96 and 130 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. '894.

Gardner et al. discloses a field effect transistor fabrication method comprising providing a thin film semiconductive layer (fig. 1A, 102; epi layer, col. 5, lines 20-26) including a channel region (fig. 1F, 118); providing a plurality of spaced semiconductive regions adjacent to the channel region of the semiconductive layer (fig. 1F, 110A & 110B); and providing a gate dielectric material over the channel region (fig. 1H, 130), providing a gate material intermediate the semiconductive regions and over the gate dielectric (fig. 1I, 136), and chemical-mechanical polishing the gate dielectric and gate material; wherein the gate dielectric has an upper surface elevationally coincident with an upper surface of the gate (fig. 1J, upper surfaces of 132A/132B are coincident with 138); and wherein the semiconductive regions comprise upper surfaces (source/drain regions 110A/B comprise upper surface layers 106A/106B) which are elevationally coincident with and in a single place of an upper surface of the gate (138).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 114 and 122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. '107 in view of Itoh et al. '595.

Itoh et al. '107 discloses all of the elements of the claims as set forth in paragraph 4 above, but the reference does not explicitly teach the emitter region to be formed by etching. Itoh et al. '595 teaches a method of forming a field emission device wherein the emitter is formed by etching (col. 1, lines 18-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the emitter of Itoh et al. '107 using the etching process of Itoh et al. '595. One would have been motivated to do this because using an etching process to form the emitter would have provided a sharp emitter tip, thus providing a large emission current and a highly reproducible structure (Itoh et al. '595, col. 1, lines 25-30).

Response to Arguments

8. Applicant's arguments with respect to the rejection(s) of claim(s) 80 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Itoh et al. '107 as set forth in paragraph 4a above.

9. Applicant's arguments with respect to the rejection of claim 79 in view of Hoffman et al. have been fully considered but they are not persuasive. Applicant argues that Hoffman et al. does not teach self-aligning a gate with a plurality of semiconductive regions. This argument is not persuasive because Hoffman et al. teaches that the emitter device (fig. 3) is used in a field emission display (col. 1, lines 20-43), which inherently has a plurality of emitters with a plurality of

semiconductive regions, and the gate (15) would be self-aligned to each of the plurality of semiconductive regions (19b).

10. Applicant's arguments with respect to the rejection of claims 83, 85, 89 and 92 in view of Itoh '107 have been fully considered but they are not persuasive. Applicant argues that the amorphous silicon layer (fig. 1, 5) under the plurality of emitters (9) does not anticipate the claimed limitation of a "semiconductive region" because layer 5 is doped to enhance conductivity. This is not found persuasive because the Applicant's own definition of the "semiconductive region" is a highly doped n+ type silicon layer (Specification, page 6, line 21 to page 7, line 4).

Applicant also argues that Figure 1 of Itoh '107 does not disclose a field effect transistor. While Itoh does not explicitly use the term "field effect transistor" to define the structure of Figure 1, this argument is not persuasive because it is well known in the art that a device having a gate (fig. 1, control electrode 3), a gate dielectric (2), a channel ("channel" region of 5), and source/drain regions (doped regions of layer 5 on either side of "channel"), and operating by applying a threshold voltage to the control gate to establish a conduction state in the channel (col. 6, line 64 – col. 7, line 6) is a "field effect transistor".

11. Applicant's arguments with respect to the rejection of claim 93 in view of Gardner have been fully considered but they are not persuasive. Applicant argues that Gardner does not teach the semiconductive regions to comprise an upper surface that is elevationally coincident with the upper surface of the gate. This argument is not found persuasive because claim 93 is written broadly enough to be anticipated by Gardner's disclosure of the semiconductive regions comprising upper

surfaces (fig. 1J, source/drain regions 110A/B comprise upper surface layers 106A/106B) which are elevationally coincident with an upper surface of the gate (138).

Allowable Subject Matter

12. Claims 74-75, 77-78, 102-106, 108-109, 111, 113, 118 and 120 are allowed.

13. Claims 81-82, 86, 128-129 and 131 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is an examiner's statement of reasons for allowance: a search of the prior art failed to disclose or reasonably suggest a method of fabricating a field effect transistor with an emitter comprising providing a gate dielectric over a channel region, providing a gate over the gate dielectric and polishing the gate dielectric and gate material to form a gate aligned with the channel region, as recited in independent claims 74 and 108. A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor with an emitter comprising providing a gate over a channel region with the use of a mask over the gate material, as recited in independent claim 102. A search of the prior art also failed to disclose or reasonably suggest a method of fabricating a field effect transistor with an emitter comprising providing a plurality of semiconductive regions adjacent a semiconductive material, one of the regions comprising an emitter, providing a gate intermediate the semiconductive regions, wherein providing the emitter comprises forming a tip of the emitter elevationally below an

upper surface of the gate and an upper surface of another one of the semiconductive regions, as recited in independent claim 118.

Itoh et al. '107, Hirano et al. '318, Kane '426, Kanemaru et al. '478, Itoh et al. '595 and Hofmann et al. '605 disclose methods of forming field effect transistors comprising an emitter formed on the drain of the transistor, but the references do not disclose the limitations set forth above.

Gardner et al. '894, Inaba '258 and Gardner et al. '025 disclose a method of forming a field effect transistor comprising a self-aligned gate formed by chemical-mechanical polishing, but the references do not disclose forming an emitter on the drain of the transistor.

15. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:30am to 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

17. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SJF

Steven J. Fulk
Patent Examiner
Art Unit 2891

March 23, 2007

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